汕头华汕电子器件有限公司

N-Channel Enhancement Mode Field Effect Transistor

HFF6N90

对应国外型号
FQPF6N90C

■ 主要用途

高速开关应用。

■ 极限值（T_a=25℃）

T_{stg}——贮存温度…… -55~150℃

T_j——结温…… 150℃

V_{DSS}——漏极—源极电压……900V

V_{GS}——栅极—源极电压…… ±30V

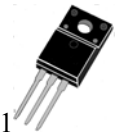
I_D——漏极电流（T_c=25℃）……6.0A

I_{DM}——漏极电流（脉冲）（注 1）……24A

P_D——耗散功率（T_c=25℃）……56W

■ 外形图及引脚排列

TO-220F



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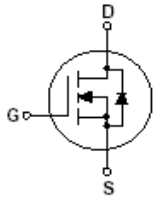
1—栅 极 G
2—漏 极 D
3—源 极 S



■ 电参数（T_a=25℃）

参数符号	符 号 说 明	最小值	典型值	最大值	单 位	测 试 条 件
BV_{DSS}	漏—源极击穿电压	900			V	I_D=250μA ,V_{GS}=0V
I_{DSS}	零栅压漏极电流			10	μA	V_{DS} =900V， V_{GS}=0
I_{GSS}	栅极泄漏电流			±100	nA	V_{GS}=±30V , V_{DS} =0V
$V_{GS(th)}$	栅—源极开启电压	2.5		4.5	V	V_{DS} = V_{GS} , I_D =250μA
$R_{DS(on)}$	漏—源极导通电阻		1.95	2.4	Ω	V_{GS}=10V, I_D =3.0A
Ciss	输入电容		1550	2010	pF	V_{DS} =25V, V_{GS}=0,f=1MHz
Coss	输出电容		145	190	pF	
Crss	反向传输电容		15	20	pF	
$t_{d(on)}$	导通延迟时间		40	80	nS	V_{DS} =450V, I_D =6.0A (峰值) R_G= 25 Ω（注 2）
tr	上升时间		120	240	nS	
$t_{d(off)}$	断开延迟时间		60	120	nS	
t_f	下降时间		70	140	nS	
Qg	栅极总电荷		35	45	nC	V_{DS} =720V V_{GS}=10V I_D=6.0A（注 2）
Qgs	栅极—源极电荷		10		nC	
Qgd	栅极—漏极电荷		13		nC	
Is	源极—漏极二极管正向电流			6.0	A	
V_{SD}	源极—漏极二极管导通电压			1.4	V	I_S =6.0A , V_{GS}=0
Rth（j-c）	热阻			2.25	℃/W	结到外壳

*注 1：漏极电流受最大结温限制。

*注 2：脉冲测试，宽度≤300μS, 占空比≤2%

■典型特性曲线

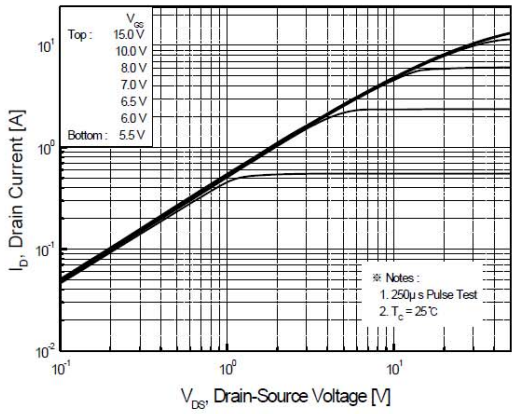


Figure 1. On Region Characteristics

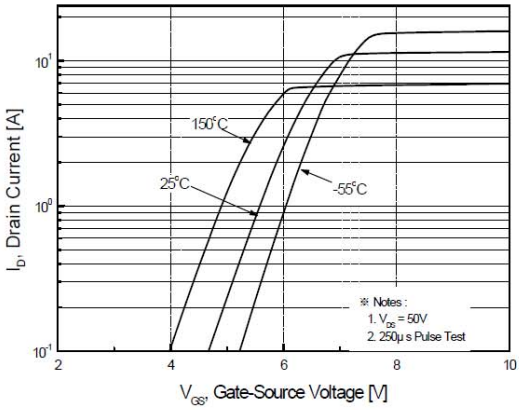


Figure 2. Transfer Characteristics

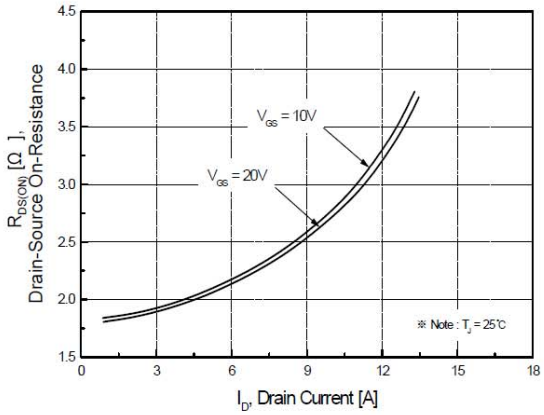


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

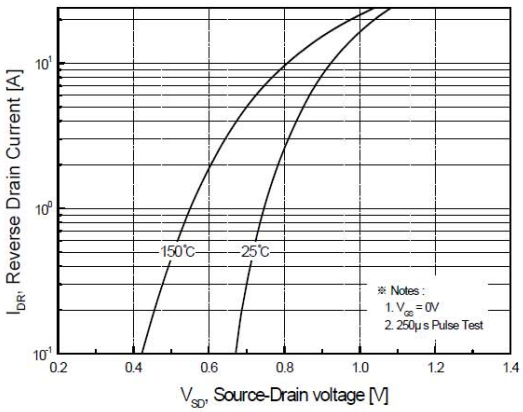


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

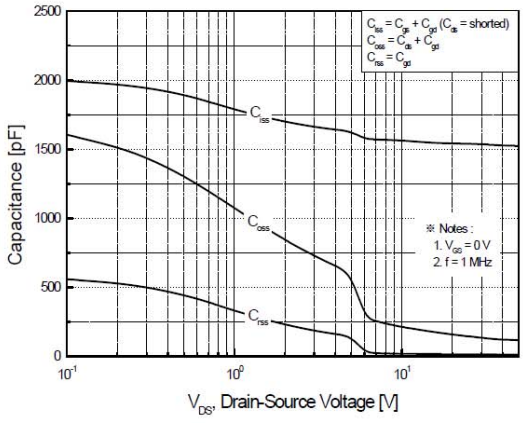


Figure 5. Capacitance Characteristics

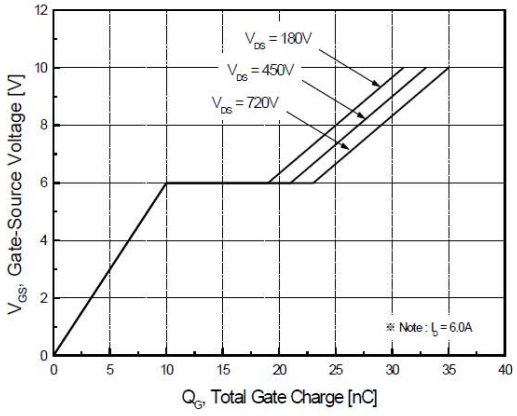


Figure 6. Gate Charge Characteristics

■典型特性曲线

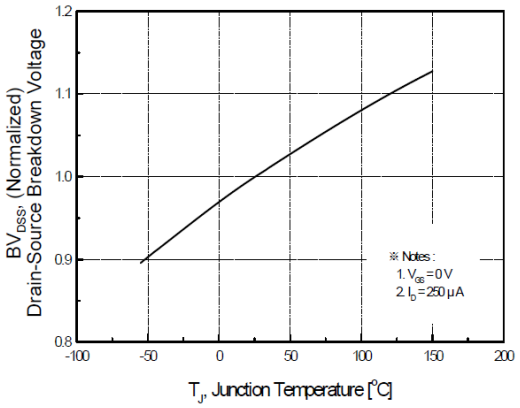


Figure 7. Breakdown Voltage Variation vs Temperature

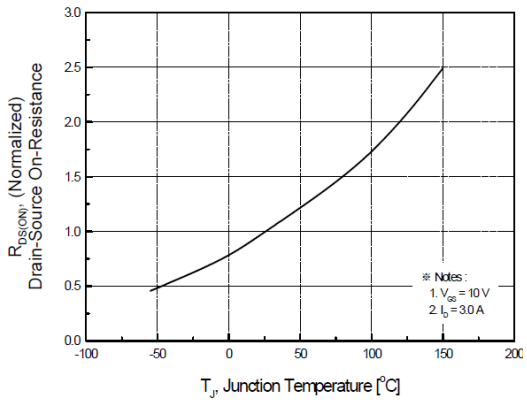


Figure 8. On-Resistance Variation vs Temperature

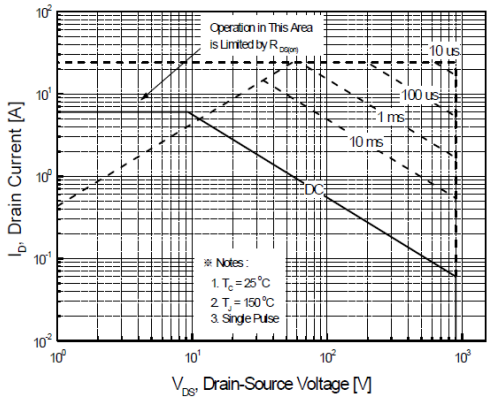


Figure 9. Maximum Safe Operating Area

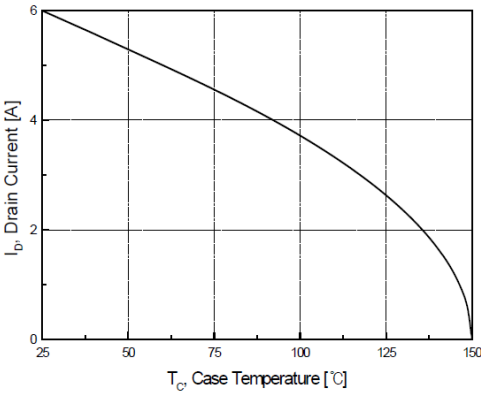


Figure 10. Maximum Drain Current vs Case Temperature

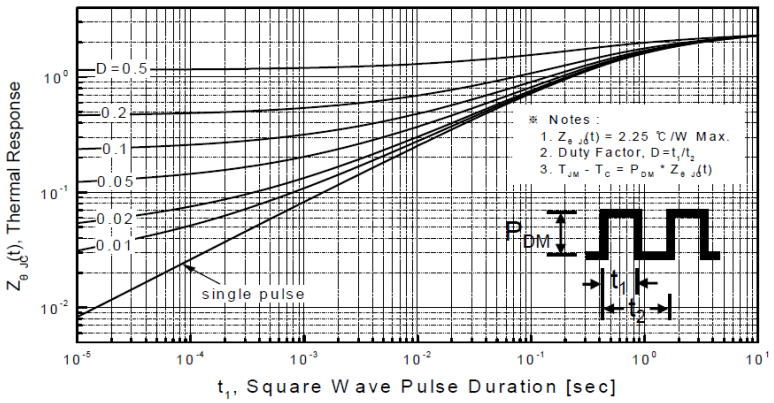


Figure 11. Transient Thermal Response Curve

■典型特性曲线

Fig 12. Gate Charge Test Circuit & Waveform

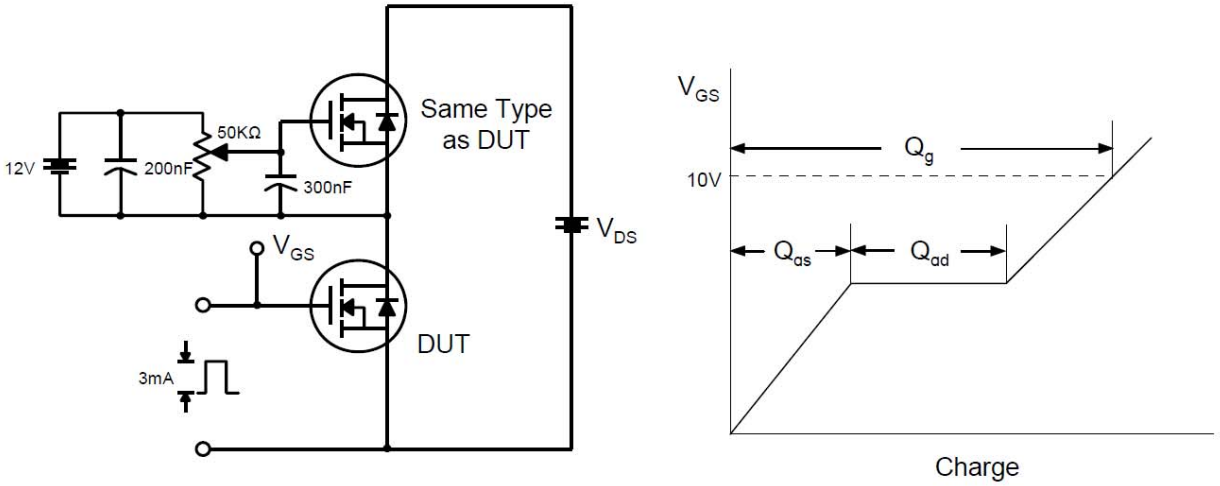


Fig 13. Resistive Switching Test Circuit & Waveforms

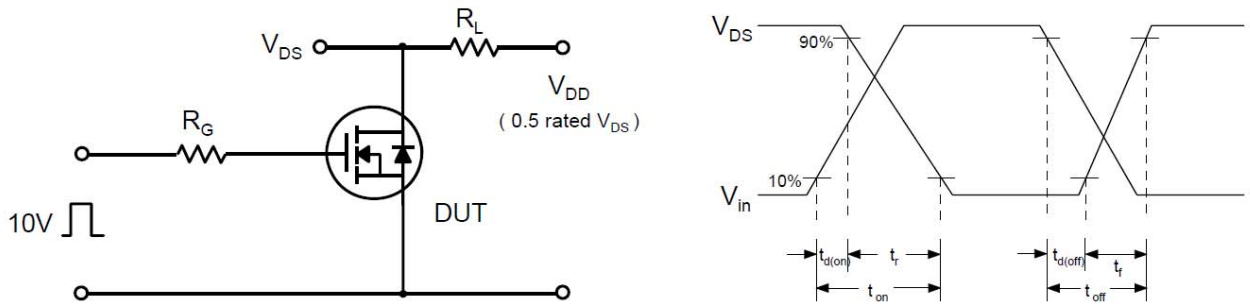
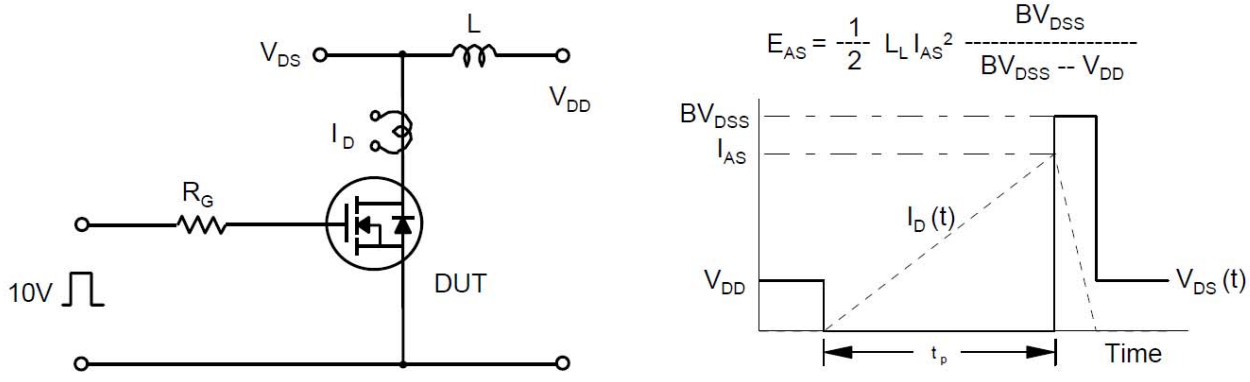


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



■ 特性曲线

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms